High Performance 45nm CMOS Technology with 20nm Multi-Gate Devices

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Outline

- **Motivation**
- Narrow ultra-thin FDSOI devices
- Performance
- Feasibility and area efficiency
- Conclusions

Motivation

- Multi-gate devices (FinFETs, tri-gates) improve device electrostatics and show promising scaling capabilities (F.-L.Yang et al, IEDM 2002, B. Yu et al, IEDM 2002, B. Doyle et al, VLSI Symp. 2003).
- Strained channels will provide performance boost for future generations (S. Thompson et al, IEDM 2002, B.H. Lee et al, IEDM 2002, K. Ota et al, IEDM 2002, T. Mizuno et al, IEDM 2002, Q. Xiang et al, VLSI Symp. 2003).
- High performance has also been achieved by using ultra-thin body and metal gates (J. Kedzierski et al, IEDM 2002, W. Maszara et al, IEDM 2002, Z. Krivokapic et al, VLSI Symp. 2003).
- The right combination of those new approaches should yield a very high performing technology (F.-L. Yang et al, VLSI Symp. 2003).

Ultra-thin FDSOI devices

A unique combination of ultra-thin SOI, undoped channel, FUSI metal gate, and selective epi yielded a high performance technology with salient features:

- Very high drive current
- Low $t_{ox,inv}$
- Lower gate leakage

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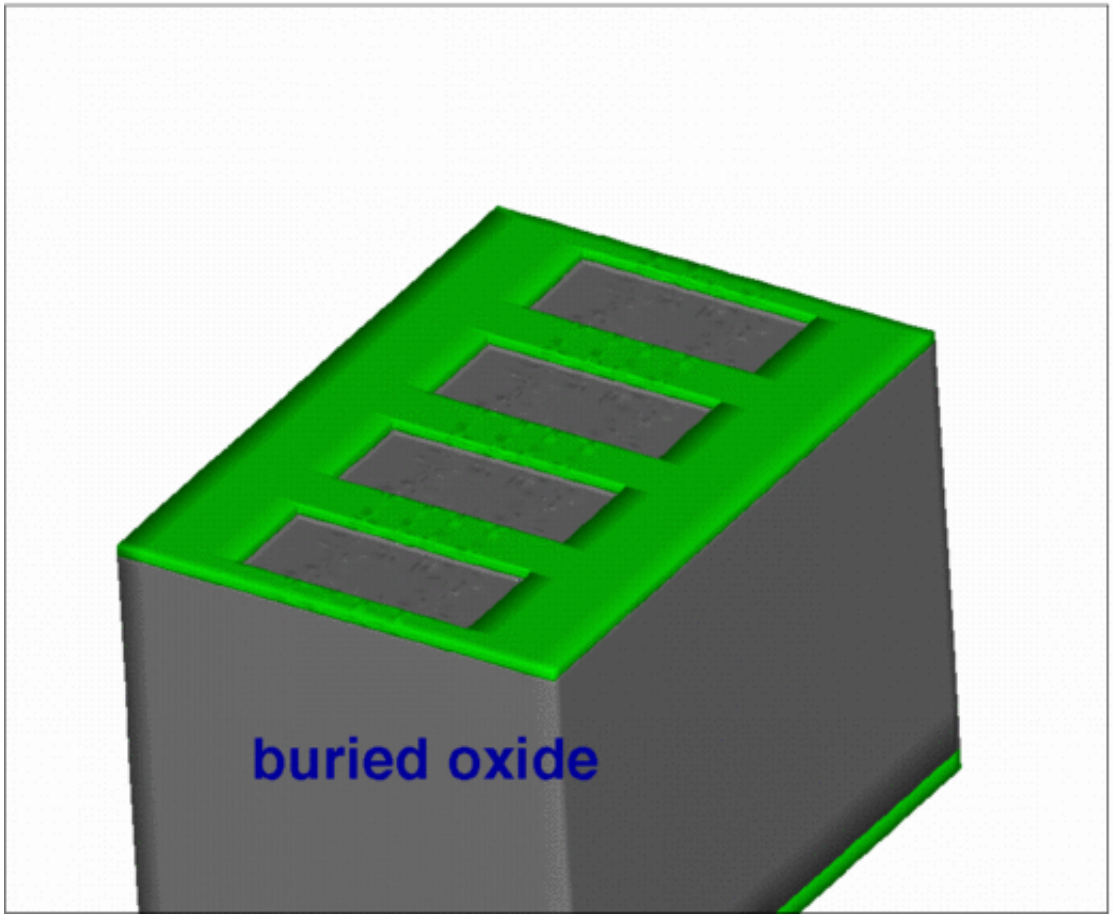
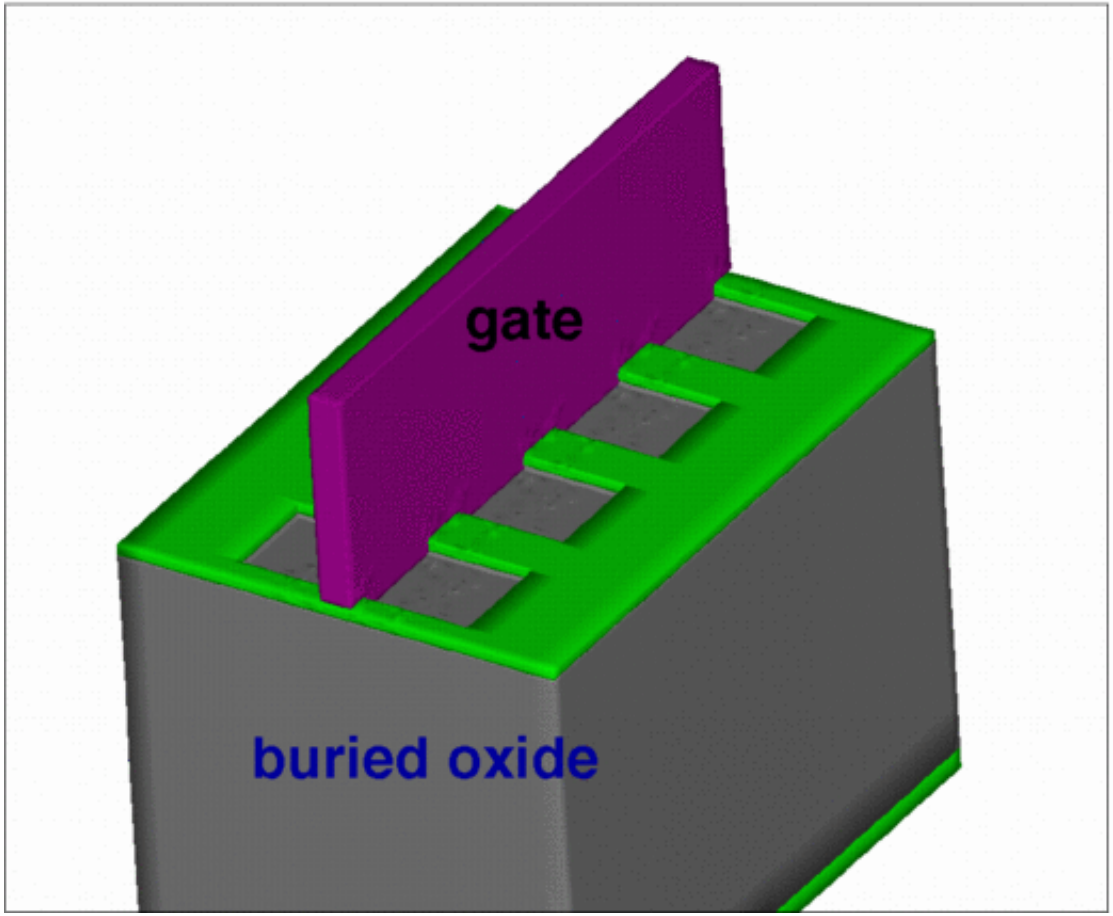
Narrow Devices

- Combination of multi-gates with mesa isolation, metal gate and SOI creates locally strained channel that significantly enhances performance.
- Phenomenon has been measured experimentally and verified by 3-D computer simulations.
- There is significant room left for performance improvement!

Narrow Device Process Flow



Narrow Device Process Flow



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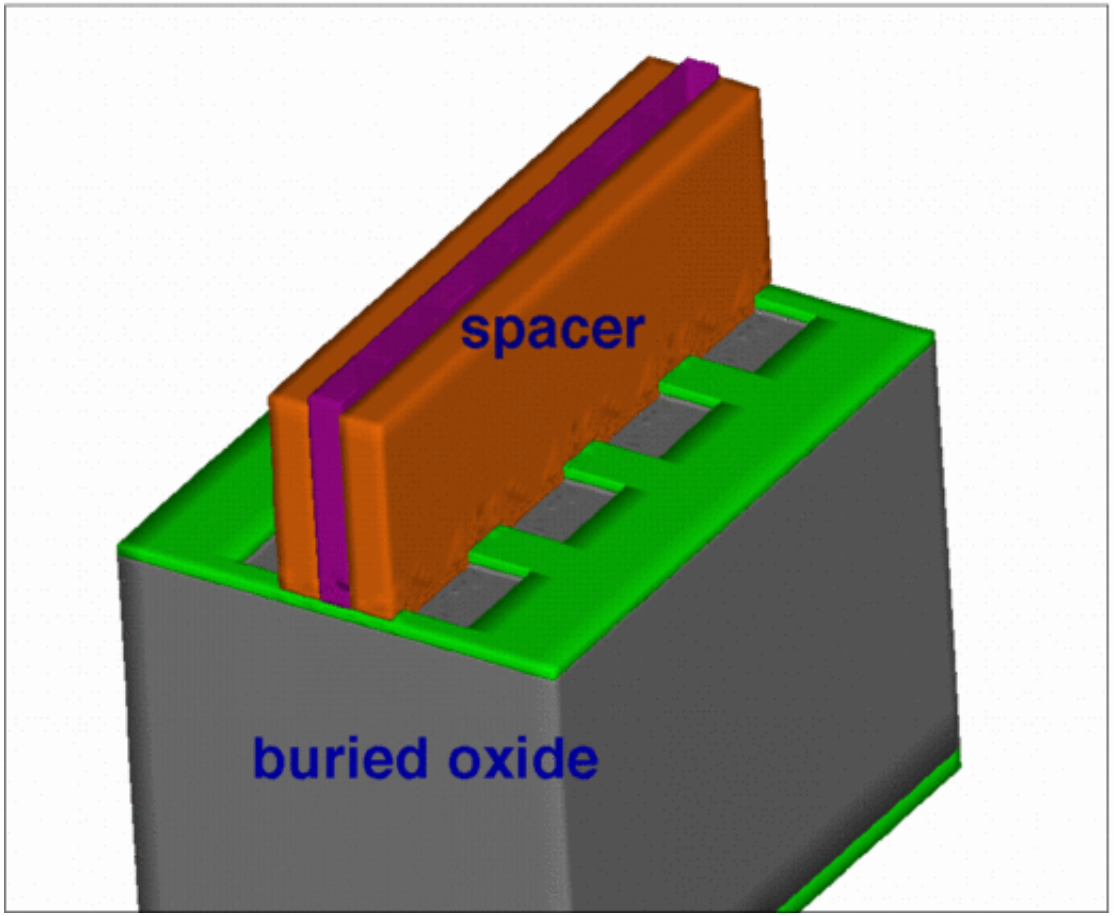

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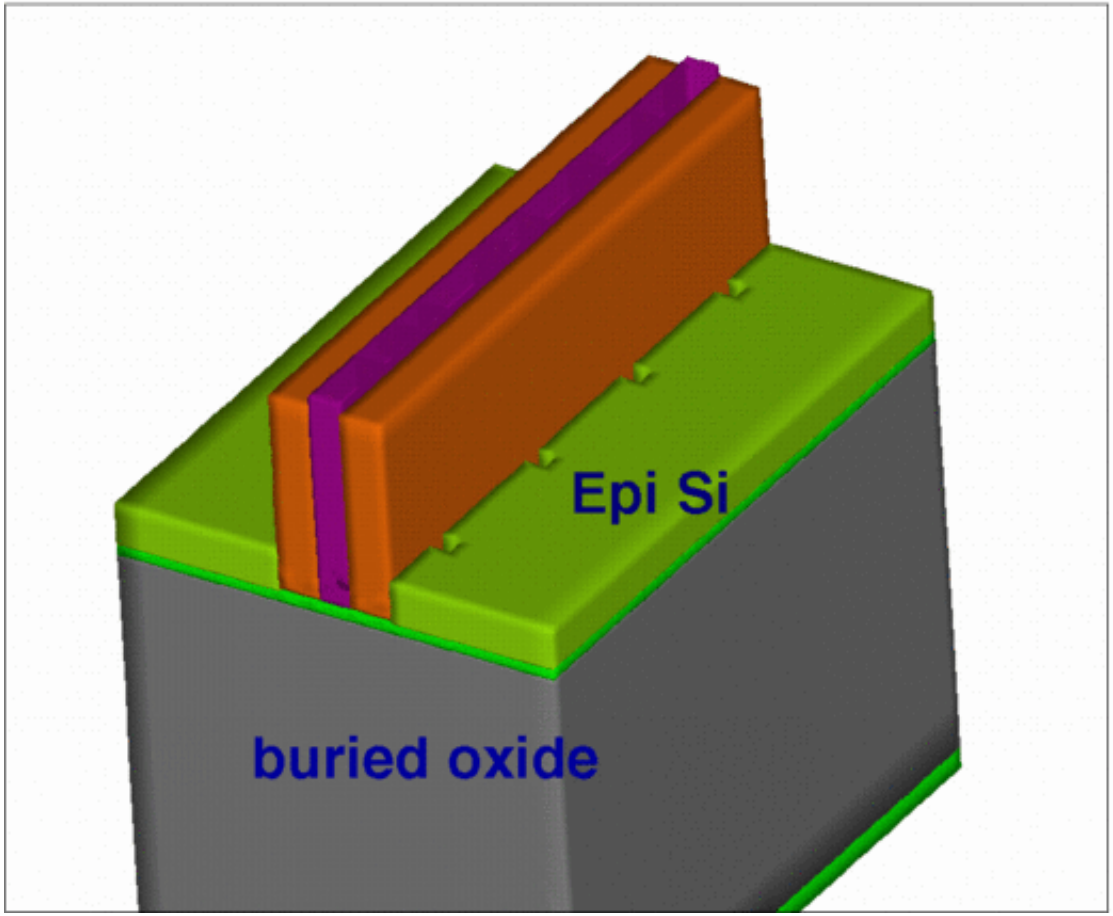

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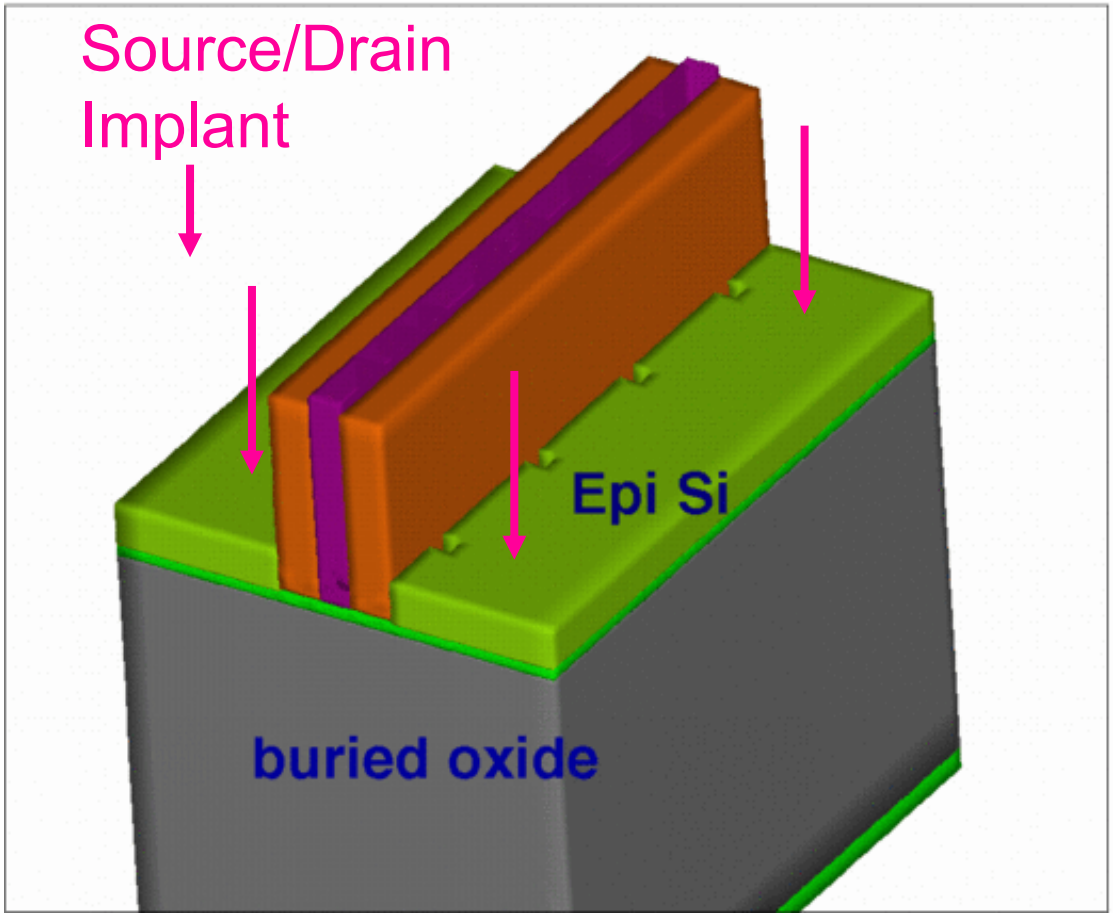
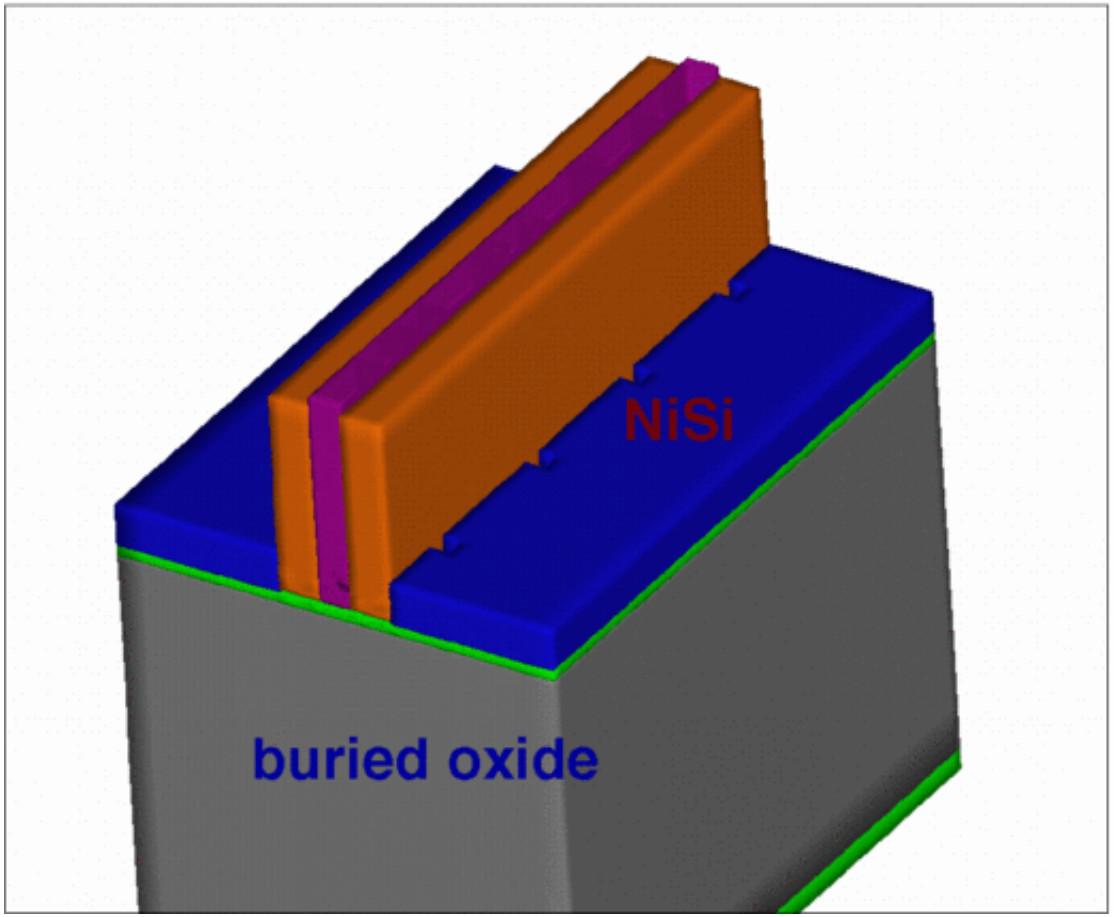
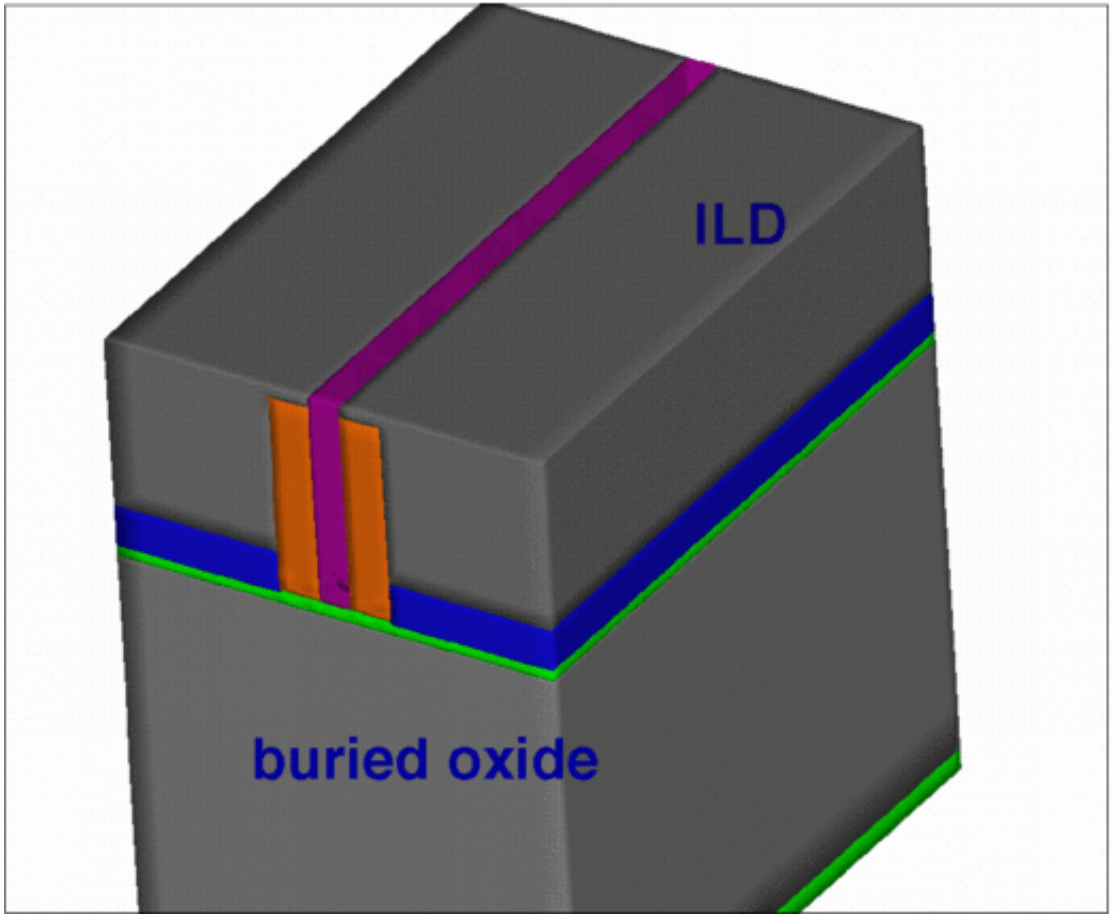


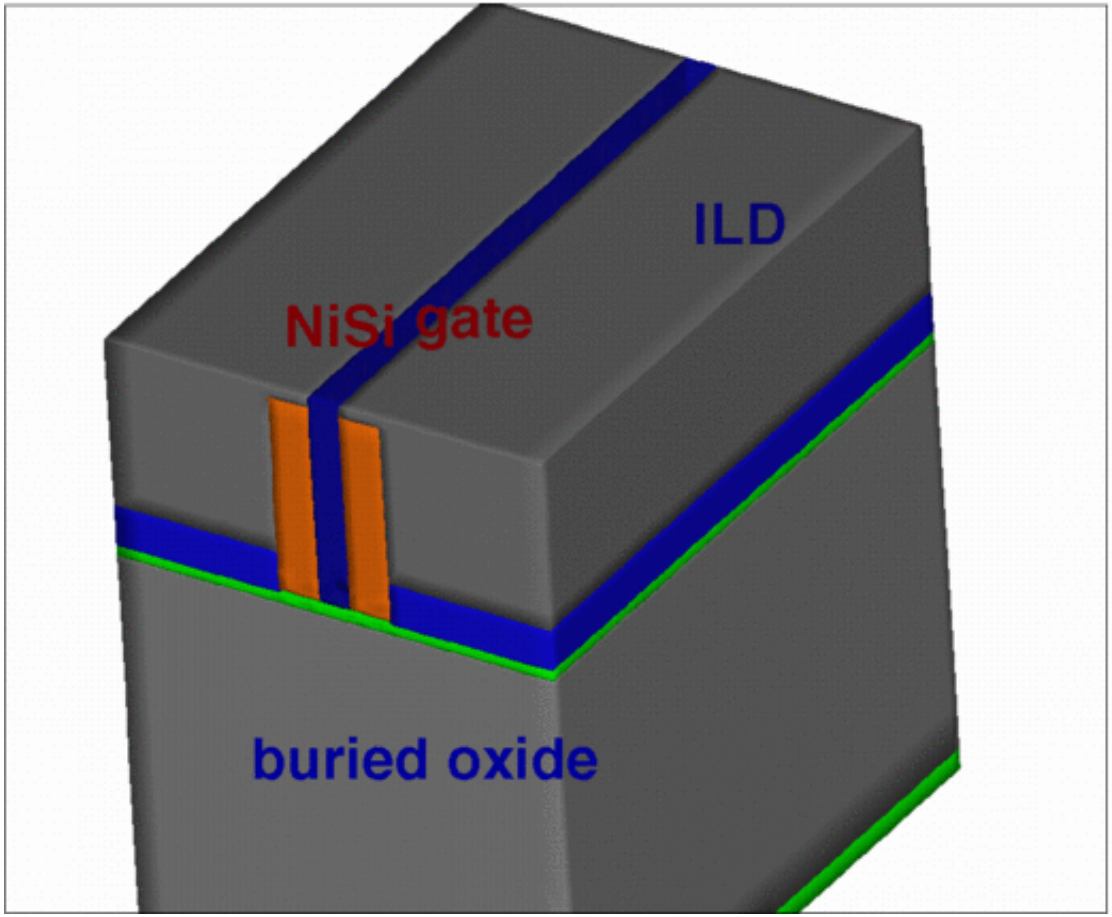
Narrow Device Process Flow



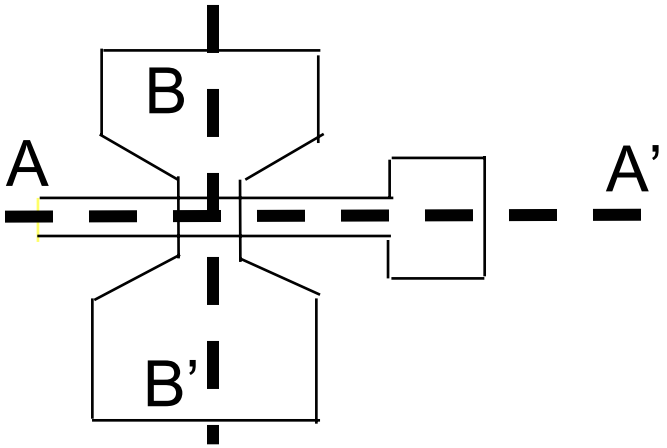
Narrow Device Process Flow



Narrow Device Process Flow



Process Details



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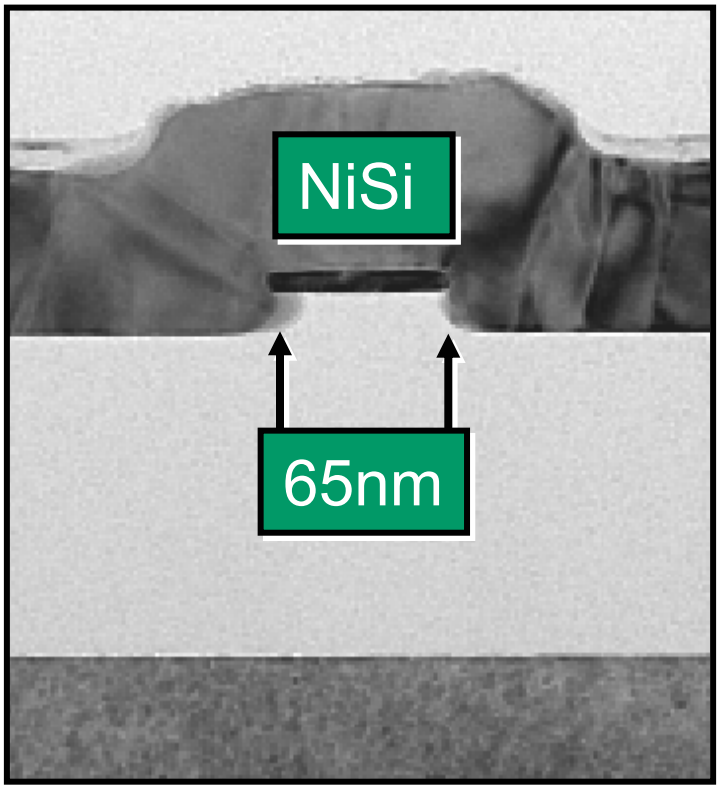

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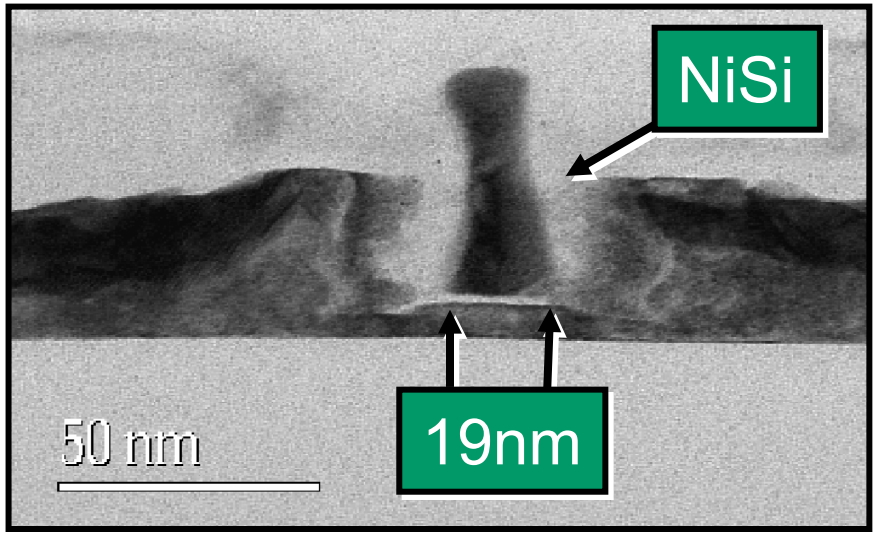

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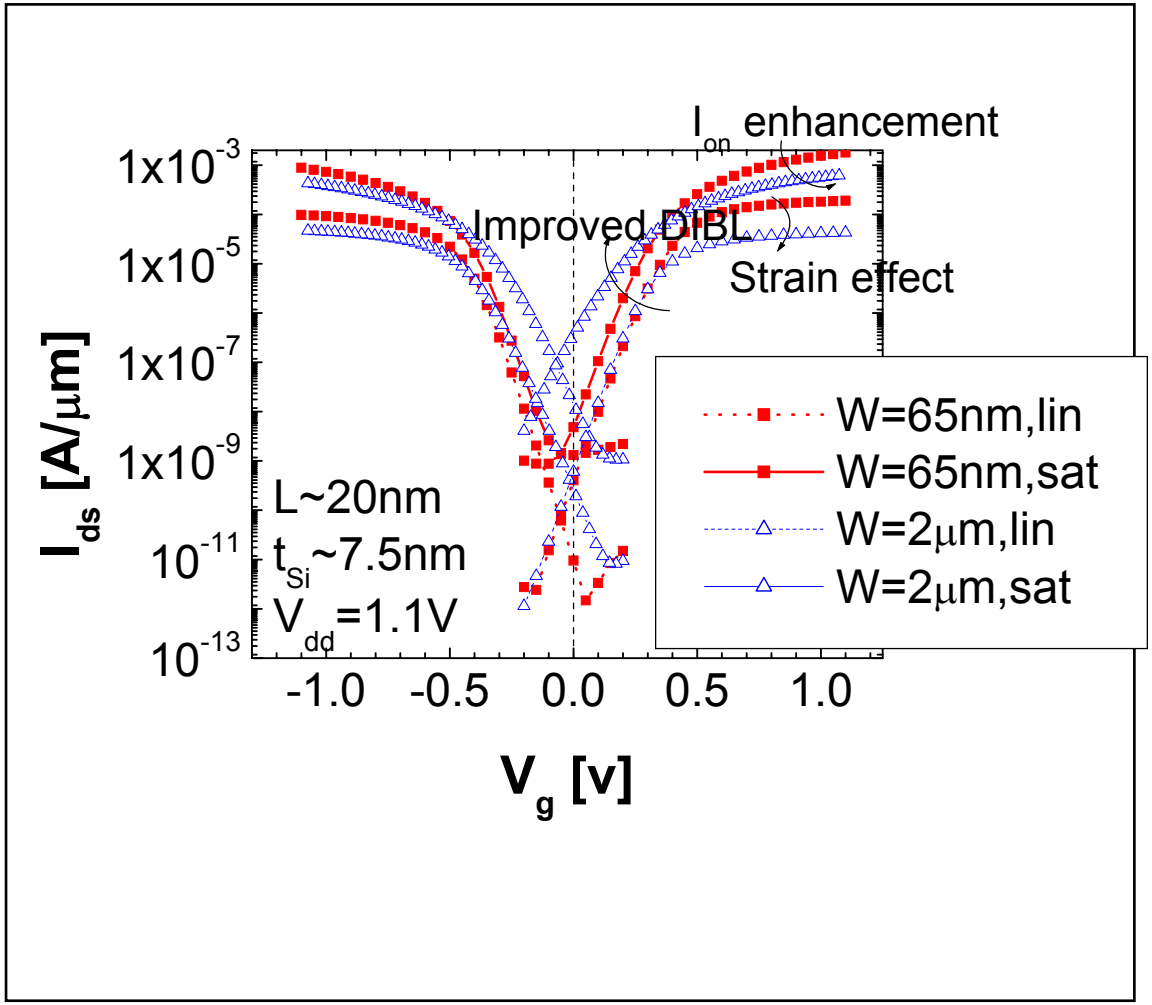
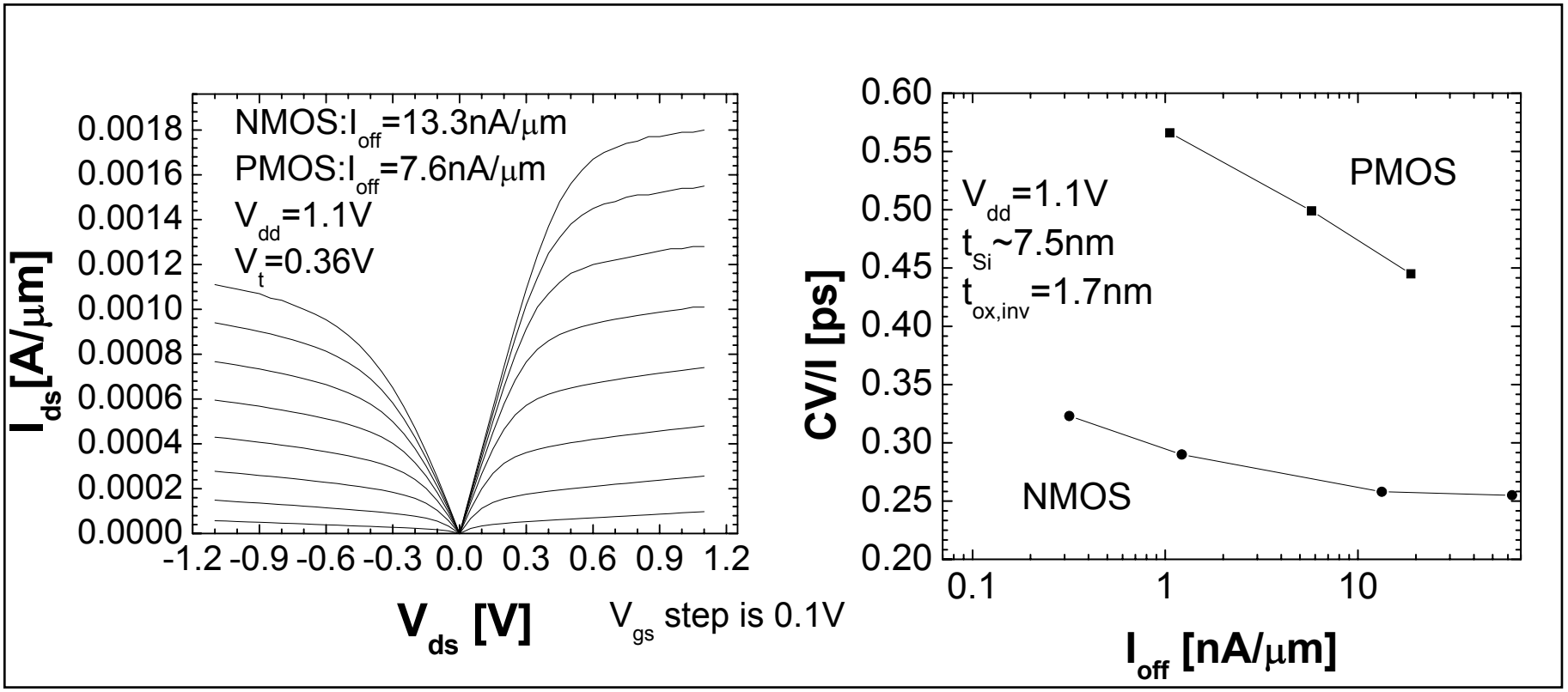
Advantages of Narrow Devices

Narrow devices have:

- Higher V_t and lower I_{off}
- Highly tensile stress compared to compressive stress for wide devices
- Larger inversion charge on the sidewalls resulting in higher I_{on}



High Performance Devices



- 80nm narrow devices achieve extremely high performance even with mid-gap work function.

Comparison with the 2003 ITRS Roadmap

	2003 ITRS Projection for 2009		AMD Multi-Gate FDSOI	
Device Parameter	NMOS	PMOS	NMOS	PMOS
Lgate [nm]	20	20	20	20
Tox,inv[nm]	1.2	1.2	1.7	1.7
Vdd [V]	1	1	1	1
Ioff [nA/um]	70	70	3.9	3.7
Ion [mA/um]	1.6	0.727	1.538	0.891
Vtsat [V]	0.16	-0.16	0.273	-0.311
S [mV/dec.]	78	78	72.7	71.6
Gm [S/mm]	2.47	1.12	2.728	1.756
jg [A/cm^2]	117	N/A	25	6
CV/I [ps]	0.48	1.05	0.23	0.39

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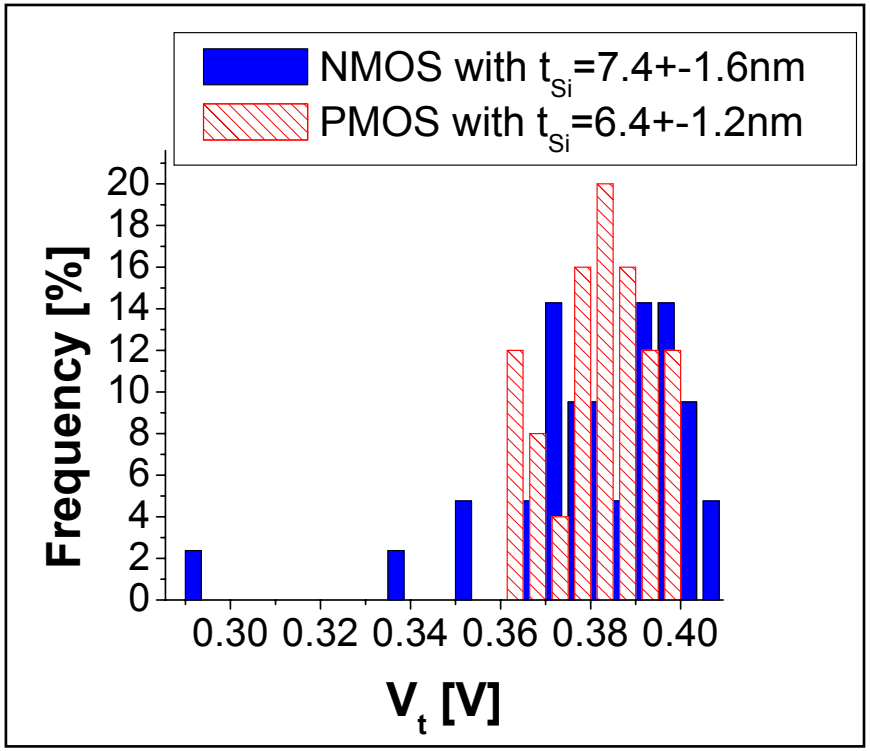
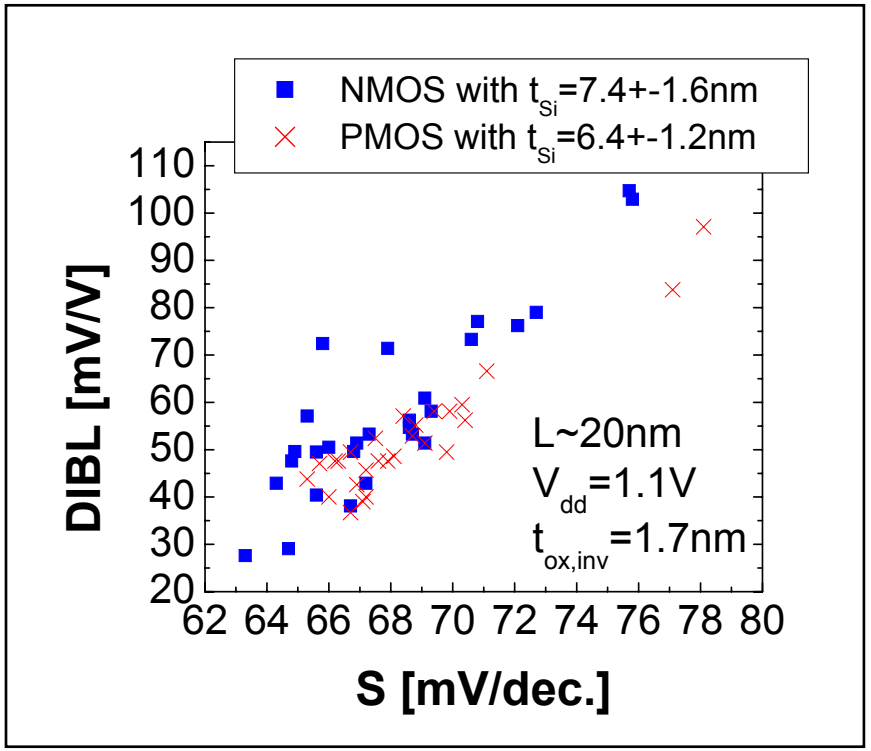
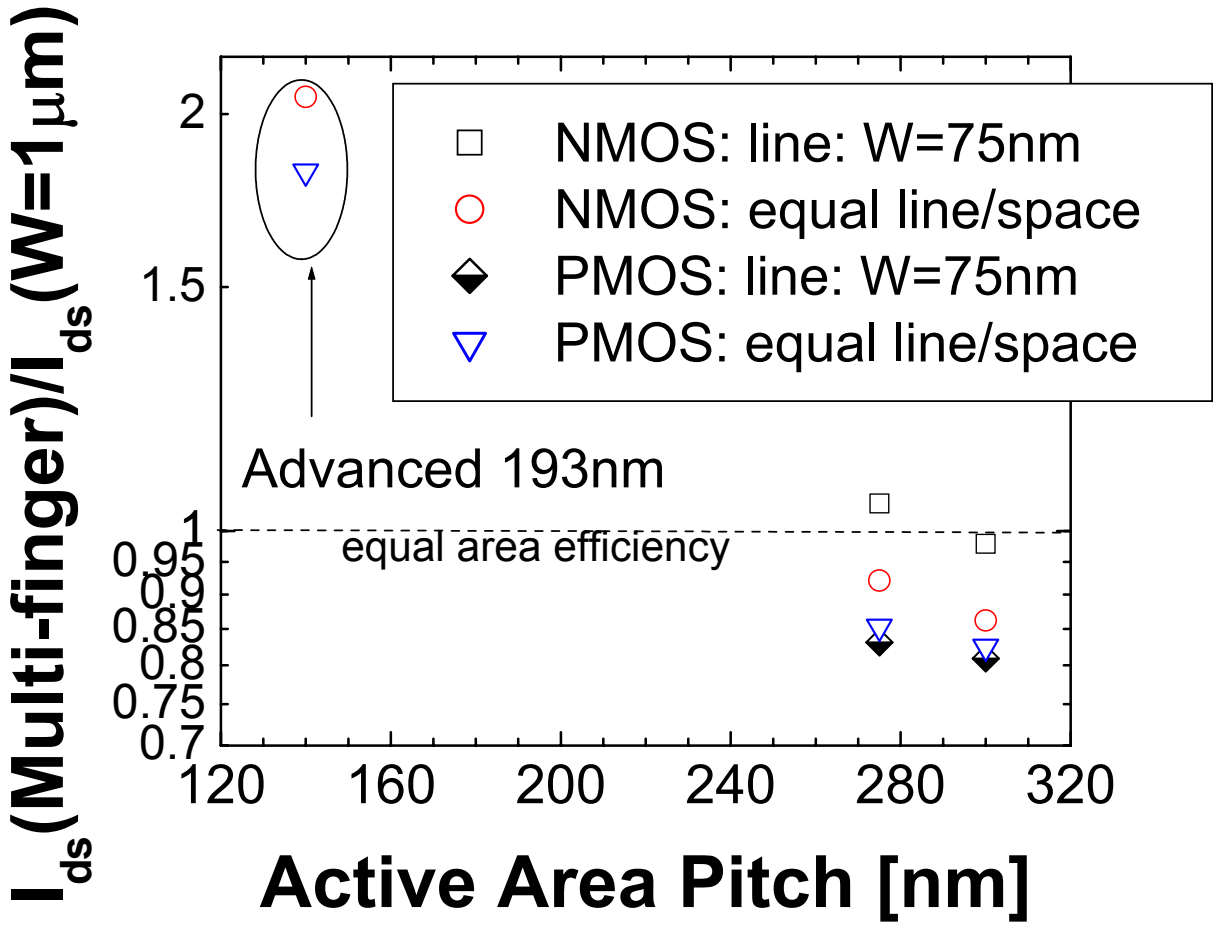
Ultra-Thin FDSOI & Manufacturability



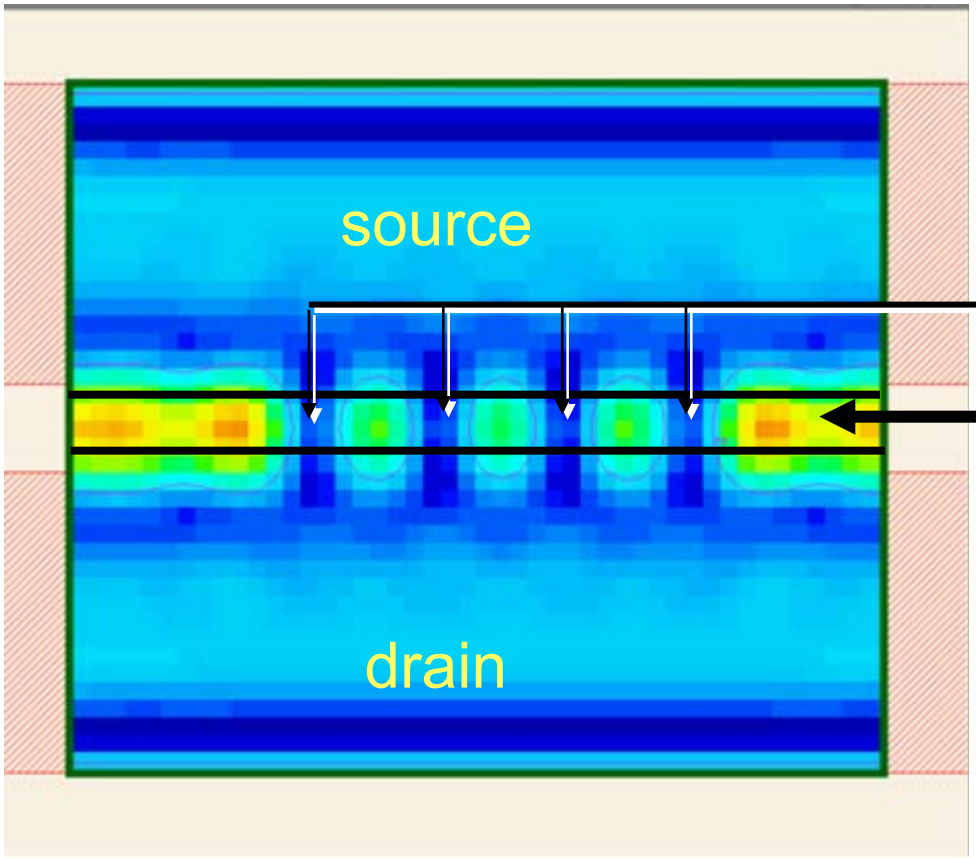


- Short channel parameters (V_t, S, DIBL) are well controlled for thinner silicon channel and better thickness control across the wafer.

Area Efficiency



Litho Requirements for Denser Fingers



193nm scanner with 0.95 NA and dipole illumination (σ_{outer}=0.85, σ_{inner}=0.55) will be able to print 140nm pitch.

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- We demonstrate that narrow FDSOI devices with ultra-thin strained channels can meet performance requirements for the 45nm technology according to the 2003 ITRS roadmap.
- We expect that such a technology will become feasible and area efficient assuming usual rate of improvement in process equipment and starting material.

Acknowledgments

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